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Silicon Precipitate Nodule-Induced Failures of MOSFETs

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ABSTRACT

Failures of power MOSFET die were caused by damage to the dielectric separating the source metallization from the gate polysilicon. These failures, which were identified during initial electrical testing, were characterized by gate-to-source shorts or diode-like curve-trace but minimal visual evidence. Liquid crystal hot spot detection was employed to identify the damage sites as small chip-outs, or *chipets*, in the dielectric. These chipets were the result of lateral displacement of silicon nodules adhering to the dielectric surface. The nodules precipitated from the 1% silicon content of the aluminum metallization.

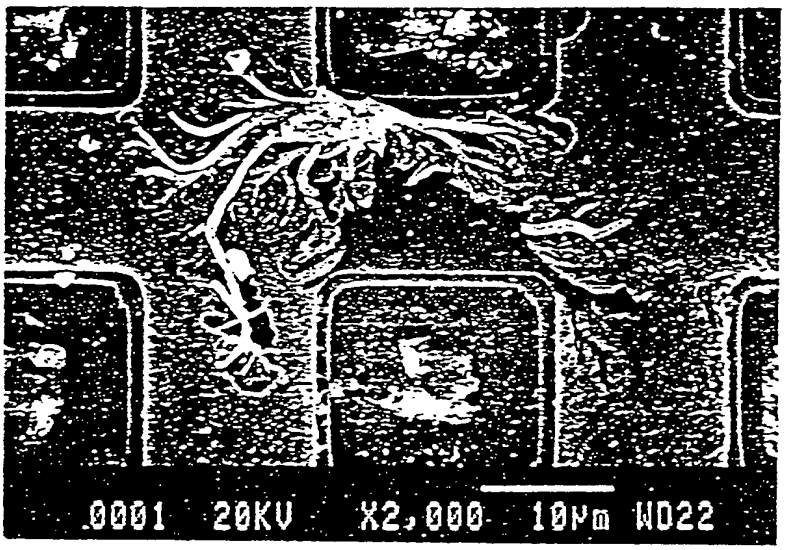

Figure 1: Unique pattern of fused polysilicon observed after removal of metallization and insulating oxide. (2000X)

TWO FAILURE MECHANISMS were identified and controlled early in the use of MOSFET die products: damage due to wirebonding, and electrical overstress, including electrostatic discharge (ESD). Wirebonding damage typically occurs when a process is not optimized for the type of die being bonded. It has a characteristic curve tracer signature common to other die fracture mechanisms: the drain-source reverse characteristic is typically leaky and unstable. This instability is believed to be due to make/break contact between the fracture faces. After chemical removal of the aluminum bond wire via hydrochloric or phosphoric acids, a fracture in the oxide beneath the bond is commonly observed. Identification of the position of the damage relative to the wire bond itself as well as the overall bond shape and appearance are important feedback for the wirebonding process team to eliminate this type of failure.

Electrical overstress (EOS) is also a common failure mechanism for power MOSFET devices. Typically, EOS failures occur after the dissipation of excessive amounts of power in the device, and frequently cause readily observable damage to the bond wires and metallization or, in more severe cases, carbonization of the molding compound. In the case of electrostatic discharge (ESD), which is actually a special case of EOS characterized by relatively high voltage but low dissipated power, a

leakage location technique like liquid crystals or photoemission must be utilized to identify the damage site, since the damage can be extremely small and may occur anywhere on the die surface. When identified, the damage site has a characteristic appearance of melted alloyed silicon and metallization, frequently appearing like a volcanic cone. Both wirebonding damage and EOS/ESD damage were experienced early in the life of this product and were controlled via Taguchi process optimization, ESD precautions, and careful review of electrical test sequences and limits.

DEVICE ANALYSIS

ELECTRICAL CHARACTERISTICS - The failures described in this paper had different electrical characteristics when tested with a curve tracer than those caused by wirebonding damage or EOS/ESD. The failures typically exhibited normal drain-source characteristics: that is, a forward diode turn-on at approximately 0.7 Volts and a reverse low leakage "open" condition until a sharp reverse breakdown, commonly in excess of 220 V[1]. I_{DSS}, or reverse leakage current measured at 200 V, was typically less than 50 nA. Thus, I_{DSS} was a poor electrical screen for these failures.

The gate-source electrical characteristics were a far better electrical screen, and gave some insight into the cause of failure. Two types of gate-source characteristics were observed: a linear resistive characteristic and a diode-like characteristic. The linear resistive characteristic typically had a resistance of a few Ohms, and led initially to the belief that the failures were due to EOS/ESD. In contrast, the diode-like gate-source characteristic, which became a hallmark of this failure mechanism, had a 0.7 V forward turn-on and high reverse leakage without a distinct reverse breakdown. Application of power levels in excess of 20 to 50 mW, as during liquid crystal hot spot detection, would frequently cause a device with a diode-like characteristic to switch to a linear-resistive one. In some cases this switch was reversible, as if a parallel fuse was being blown out by the applied current.

[1]It is important to note that for MOSFET devices all two-terminal curve characteristics (e.g. drain-to-source or gate-to-source) assume that the third terminal is externally shorted to the source terminal. Commonly, the drain-to-source leakage current is abbreviated IDSS to indicate that the gate terminal is shorted to the source.

LIQUID CRYSTAL HOT SPOT DETECTION - Among the techniques used to identify the locations of leakage in MOSFETs, perhaps the easiest and most commonly used is liquid crystals (LC). A nematic liquid crystal material with a +30°C transition temperature was used in this analysis, and no external temperature controller was employed. Because the gate-to-source characteristic was normally affected, these terminals were energized via a probe station and curve tracer to produce the power dissipation necessary for the technique to operate.

Initial liquid crystal analysis indicated that the damage sites were located beneath one or more of the source wire bonds. Fairly high power dissipations were employed, averaging in excess of 50 mW. The passivation and metallization were removed by immersing the device in HCl in an ultrasonic bath. The acid dissolves the aluminum metallization under the passivation beginning at the bondpads, allowing the passivation to flake off. This exposed the underlying oxide layer.

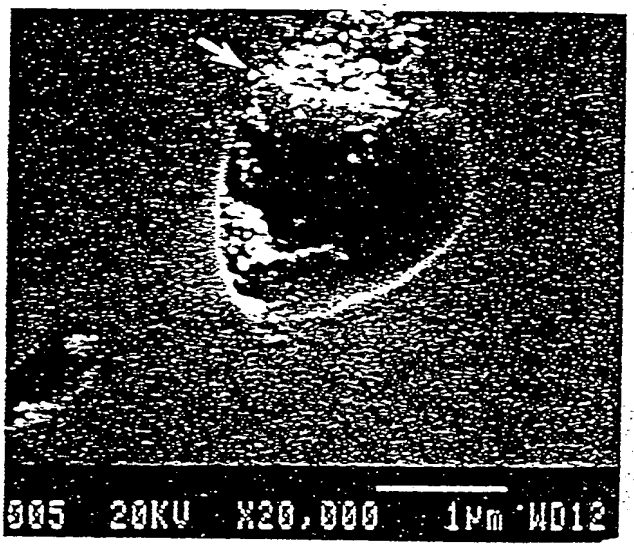

Figure 2: Small electrical damage site within chipet. (25000X)

Subsequent optical inspection identified an apparent electrical damage site under the wirebond. This damage was characterized by a central fused-site surrounded by multiple filaments (Figure 1). These filaments were dubbed "tentacles" or "roadkill" damage because of their appearance. SEM inspection of the same locations revealed surprisingly little

detail, indicating that the filaments were located beneath the surface of the exposed oxide layer. The oxide was then chemically etched with buffered hydrofluoric acid to expose the gate polysilicon layer beneath. An extensive pattern of filamentation in the polysilicon was observed with optical and SEM inspection. The filaments radiated from a central site, or nucleus, normally on the edge of a MOSFET cell, and extended across many square microns of the surface. These filaments could be readily observed using a medium power (50X) optical microscope.

Cross-sections of failures revealed that the filaments were confined to the polysilicon layer, except at the central nucleus. At the nucleus, melted silicon and aluminum were observed extending vertically through the dielectric layer. On several devices where the filamentation was minimal, there was limited evidence of melting at the nucleus site and a small section or chip of the dielectric was missing (figure 2).

To determine whether some form of corrosion was responsible for the growth of the filaments, Auger microprobing was utilized to map the elemental composition of a damage site as well as the surrounding area. Care was taken to minimize contamination of the area during handing. Auger did not detect the presence of any unexpected elements, such as light cations or anions.

It is now believed that the filaments are the result of amplification of the damage at the original failure sites by the application of excess power during liquid crystal testing. A slightly higher level of power was necessary to counteract the obstructing heatsink effect of the relatively large wirebond. The heat generated at the damage site would initiate crystallization of the amorphous polysilicon depending on the amount of power dissipated. If the applied power during LC testing was maintained at 25 mW or less, little or no filament growth would occur. Deliberate "decoration" of the damage site by generating filamentation was a useful albeit destructive technique to simply confirm the presence of this failure mechanism since it requires only a readily available medium power optical microscope to locate the damage site.

Figure 3: Silicon precipitates (nodules) viewed from side exhibit variety of shapes and sizes. (12700X)

CHARACTERISTICS OF NODULES

Since cross-sections and SEM analysis implicated abnormally large chipouts in the insulating oxide, the silicon precipitates -- known to cause similar damage -- were studied in greater detail. These precipitates, or nodules, form either at the surface of the underlying oxide or remain suspended within the metallization layer. The ratio of adhered and suspended nodules was seen to vary widely. The suspended nodules, while observable in cross-section, are washed away by chemical etching of the aluminum. The remaining adhered nodules vary in size and shape. Although they appear roughly circular under high power microscopy (400X), they are actually polyhedral and exhibit a wide range of aspect ratios (Figure 3). Typical height/width ratios range from 0.3 to 1.8.

There were typically 50×10^3 to 100×10^3 nodules per square millimeter in the subject devices. In general, the nodule density -- the number of nodules per unit surface area -- was inversely proportionate to the average size of the nodules. That is, when the nodules were large, there tended to be few of them. Conversely, when the nodule count was high, they tended to be small. Figure 4 shows a typical histogram of nodule sizes produced by an image analysis

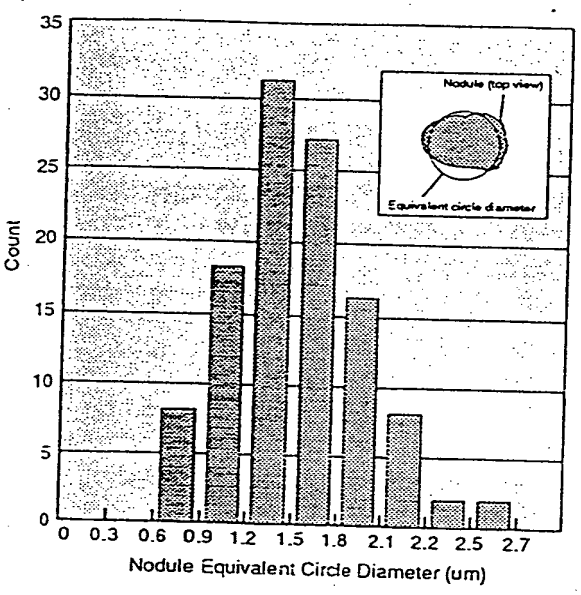

Figure 4: Example distribution of nodule sizes

system capable of performing feature counting. Unfortunately, easily measured characteristics of the nodules, such as density (count/area), could not be easily correlated to failure rate. It is hypothesized that the probability of failure is governed by extreme value statistics (weakest link theory), and detailed info regarding the shape and size of the nodules can be difficult to obtain on a large number of samples.

THE NODULE/CHIPET FAILURE MECHANISM

As is widely practiced in the semiconductor industry, the aluminum metallization of the MOSFET is doped with 1% silicon to avoid junction spiking in the contacts. The silicon precipitates out of the aluminum, usually along grain boundaries, and coalesces into nodules during cooling after deposition [7]. This process is driven by the low solid solubility of silicon in aluminum below 200°C. Subsequent thermal process steps, such as anneals and passivation deposition, have the effect of increasing nodule size as the silicon is further segregated and large nodules grow by absorbing small ones [6].

The adhered nodules could be removed quite easily; gentle brushing of a few fibers from a cotton swab was sufficient to disturb them. When these well-adhered nodules are displaced, they often take with them a portion of underlying oxide, forming a distinctive, football-shaped chip-out, or *chipet* (Figure 5). The depth of the resulting chipet was roughly equal to half the length of the chipet's minor axis, itself related to the area of contact between nodule and oxide.

Earlier references to nodules as causes for failure focussed on their role as stress risers in integrated circuit devices [1], [2], [3] or by causing open interconnects [4], [5]. The chipet as stress riser initiated a fracture under the gold ball-bond which then propagated, finally resulting in complete separation of the bond and its underlying silicon from the pad, or cratering. As a cause of opens, nodules the width of an interconnect caused the line to separate. In these failures the damage was latent and only occurred after subsequent thermal stress.

In the MOSFET devices the lateral displacement of the nodules occurs during the wirebonding process. The cavity formed by the chipet is immediately filled with aluminum. These chipets, during

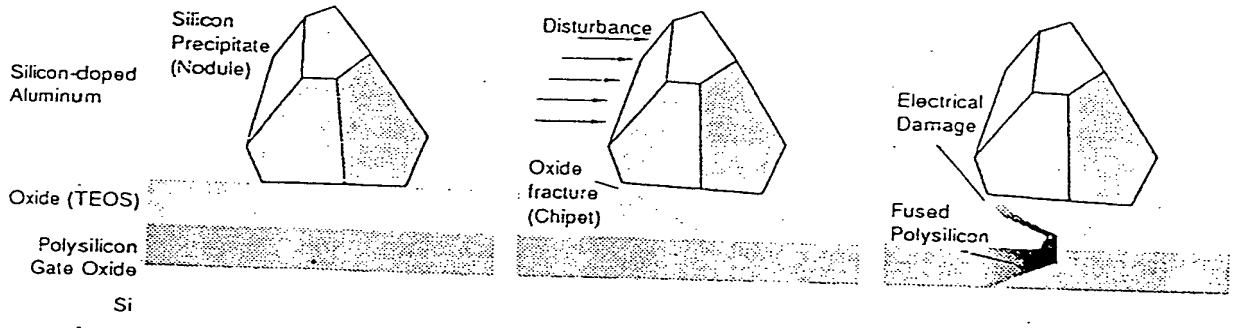

Figure 5: Movement of nodule results in fracture of underlying oxide.

electrical stress, appear to act as weak points in the insulating oxide. If the chipet is sufficiently deep to fully compromise the thickness of the dielectric oxide, a linear resistive short between the source metallization and gate polysilicon results. However, if the root only partially compromises the dielectric, a leaky diode-like characteristic results.

CONCLUSION

A failure mechanism for power MOSFET devices was identified as mechanical damage to the dielectric layer separating the source metallization from the polysilicon gate. This damage occurs because of the displacement during wirebonding of silicon precipitate nodules adhering to the dielectric surface.

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